High Power Factor Flyback PWM Controller

GENERAL DESCRIPTION

WT6679 is a high power factor flyback PWM controller special for lighting applications.

WT6679 features an internal start-up timer for stand-alone applications, an analog multiplier with for power factor correction (PFC), zero current detector (ZCD) to ensure TM operation, a current sensing comparator with built-in leading-edge blanking, and a totem pole output ideally suited for driving a power MOSFET.

WT6679 offers great protection coverage including system VCC under voltage lockout (UVLO),VCC over voltage protection, Cycle-by-cycle current limiting, and gate drive output clamping for external power MOSFET protection.

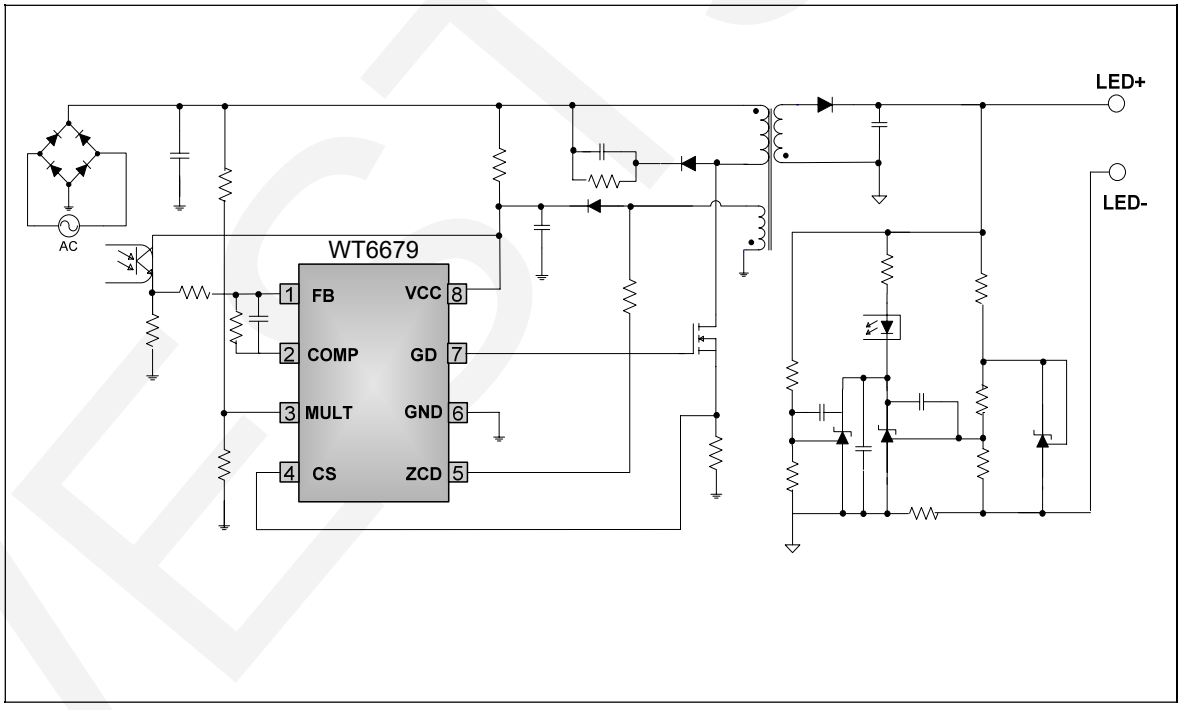
FEATURES

- Low Start-up Current and Operating Current
- Cycle-by-Cycle Current Limiting
- Internal Leading Edge Blanking
- Analog multiplier for Power Factor Correction
- Internal Startup Timer for Stand-alone Applications
- Trimmed 1.5% Internal Band gap Reference
- Under Voltage Lockout with Hysteresis
- VCC over voltage protection
- Transition Mode (TM) Operation
- Totem Pole Output with High State Clamping
- Audio Noise Free
- 11V to 32V wide range of VCC voltage

APPLICATIONS

- Single Stage High PF Flyback AC/DC SMPS
- LED Lighting Power

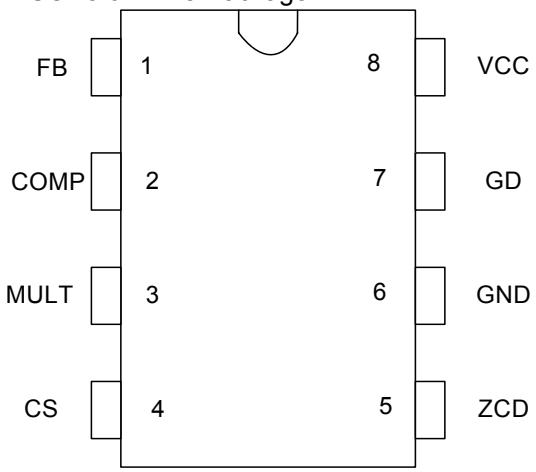
TYPICAL APPLICATION



GENERAL INFORMATION

Terminal Assignment

In SOP8 or DIP8 Package.



Ordering Information

Part Number	Description
WT6679D	8Pin DIP, Pb free in Tube
WT6679S	8Pin SOP, Pb free in Tube
WT6679E	8Pin SOP, Pb free in T&R

Package Dissipation Rating

Package	RθJA (℃/W)
DIP8	90
SOP8	150

Absolute Maximum Ratings

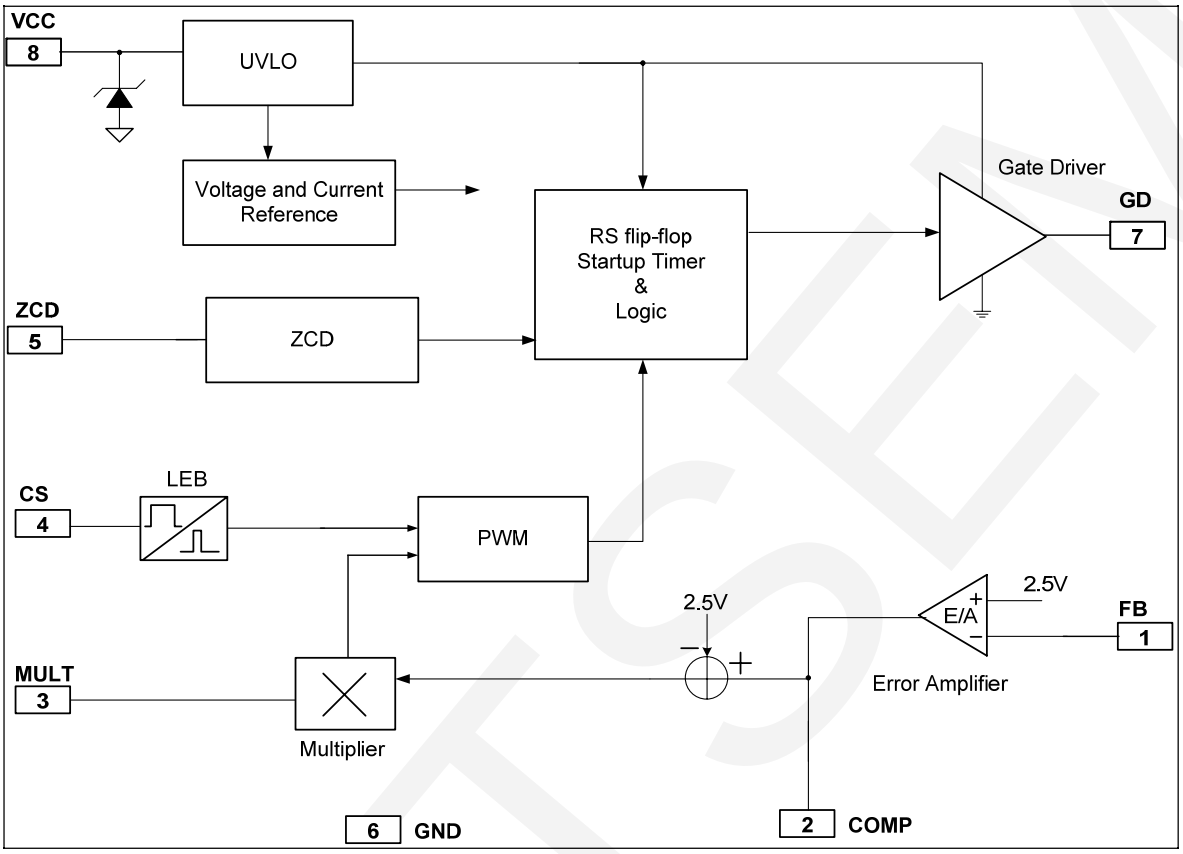
Symbol	Parameter	Value
VCC	DC Supply voltage	Vz
I_ZCD	Zero Current Detector Max. Current	50mA(source) -10mA(sink)
CS FB COMP MULT	Analog inputs & outputs	-0.3 to 7V
Tj	Maximum Operating Junction Temperature	150 ℃
Tstg	Min/Max Storage Temperature	-55 to 150 ℃
Lead Temperature	(Soldering, 10secs)	260 ℃

Note: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

TERMINAL DESCRIPTIONS

Pin Num	Pin Name	I/O	Description
1	FB	I	Input of error amplifier.
2	COMP	O	Output of error amplifier. A feedback network is placed between FB and the COMP pin. The voltage of COMP and pin 4 generate PWM duty cycle.
3	MULT	I	Input of multiplier. Connected to line voltage after bridge diodes via a resistor divider to provide sinusoidal reference voltage to the current loop.
4	CS	I	Current sense input pin. Connected to MOSFET current sensing node.
5	ZCD	I	Zero Current Detection input. When activated, A new switching cycle starts. If it is connected to GND, the device is disabled.
6	GND	P	Ground pin
7	GD	O	Gate driver output. Drive power MOSFET.
8	VCC	P	DC supply voltage.

BLOCK DIAGRAM

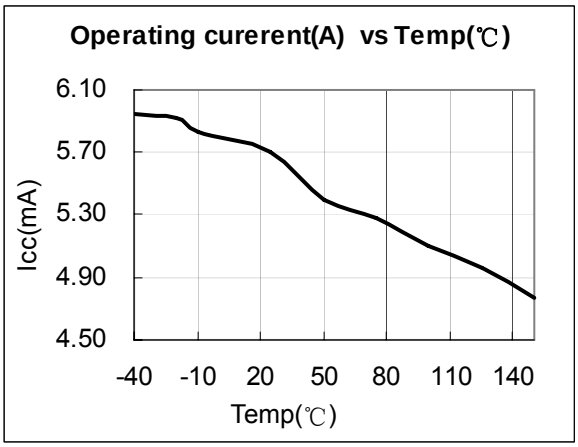


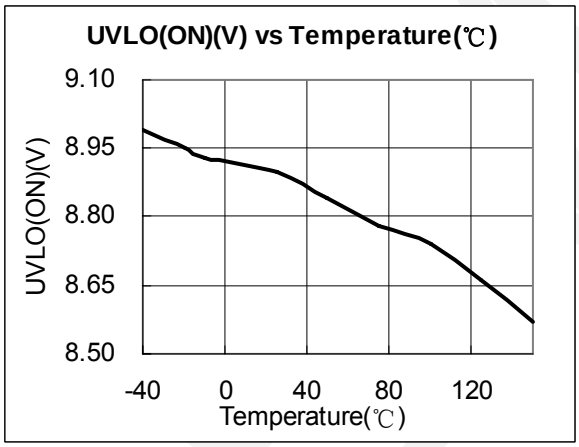
ELECTRICAL CHARACTERISTICS

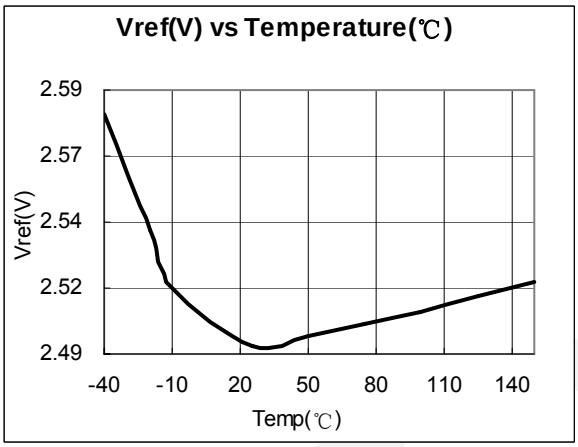
(T_A = 25℃ if not otherwise noted)

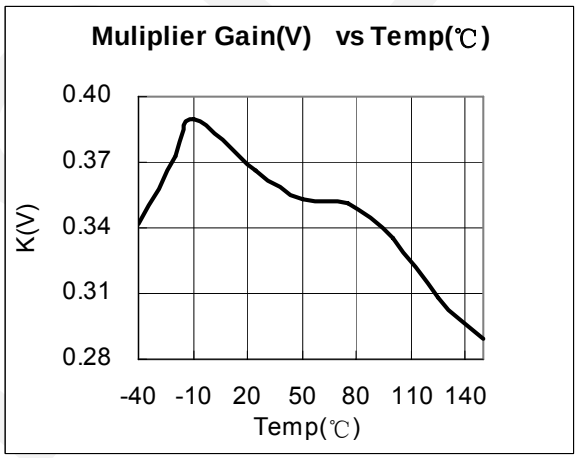
Symbol	Pin	Parameter	Test Conditions	Min	Typ	Max	Unit
SUPPLY VOLTAGE SECTION							
Vcc	8	Operating Range	After Turn On	11		32	V
UVLO(OFF)	8	VCC under voltage lockout exit		15.5	16.5	17.5	V
UVLO(ON)	8	VCC under voltage lockout enter		8.0	8.8	9.6	V
Hys	8	Hysteresis			7.7		V
Vz	8	VCC Zener Clamp Voltage	Icc=5mA		38		V
Vcc_ovp	8	VCC OVP threshold			36.5		V
SUPPLY CURRENT SECTION							
Icc-start	8	Start-up Current	Vcc=11V		5	15	uA
Iq	8	Quiescent Current, No Switching	Vcc=14.5V		1.8	3	mA
Icc	8	Operating Supply Current	GD=1nf @ 70kHz		5	7	mA
ERROR AMPLIFIER SECTION							
VREF	1	EA Reference	V_{cc}=14.5V	2.45	2.5	2.55	V
Gv		Voltage Gain	Open Loop	60	80		dB
Gb		Gain Bandwidth			1.2		MHz
ICOMP	2	Source Current	COMP=3.6V, FB=2.4V	-2	-6	-10	mA
		Sink Current	COMP=3.6V, FB=2.6V	2	6	10	mA
VCOMP	2	Upper Clamp Voltage	Isource=0.5mA		4.9		V
		Lower Clamp Voltage	Isink=0.2mA		2.25		V
MULTIPLIER SECTION							
Vmult	3	Linear Operating Range	COMP=3.0V	0 to 3.5			V
ΔVcs/ ΔVmult		Output Max. Slope	Vmult=from 0 to 0.5V, COMP=4.9V	0.95	1.1		V/V
K		Gain	Vmult=1V, COMP=3.5V	0.28	0.36	0.44	1/V
CURRENT SENSE COMPARATOR							
Vcs	4	Current Sense Reference Clamp	Vmult=2.5V COMP=4.9V	0.94	1.0	1.06	V
Td(H-L)	4	Delay to Output			200	450	ns
ZERO CURRENT DETECTOR							
Vzcd	5	Input Threshold Voltage Trigger level			0.25		V
Vzcd_hys		ZCD trigger Hysteresis			0.75		V
Vzcd	5	Upper Clamp Voltage	Izcd=2.5mA	5.1	5.7	6.3	V
Vzcd	5	Lower Clamp Voltage	Izcd=-2.5mA		0		V
Izcd	5	Source Current Capability		-3		-5	mA
Izcd	5	Sink Current Capability		3		10	mA
STARTUP TIMER							
Tstart		Re-Start Timer Period		45	55	65	us
GATE DRIVE SECTION							
VoL	7	Low Output Voltage	Vcc=14.5V, Io=100mA			1.5	V
VoH	7	High Output Voltage	Vcc=14.5V, Io=100mA	8			V
Tr	7	Rising Time	Cl=1000pF, 10~90%		80	150	ns
Tf	7	Falling Time	Cl=1000pF, 10~90%		30	70	ns
Voclamp	7	Output Clamp Voltage	Vcc=28V		16	18	V

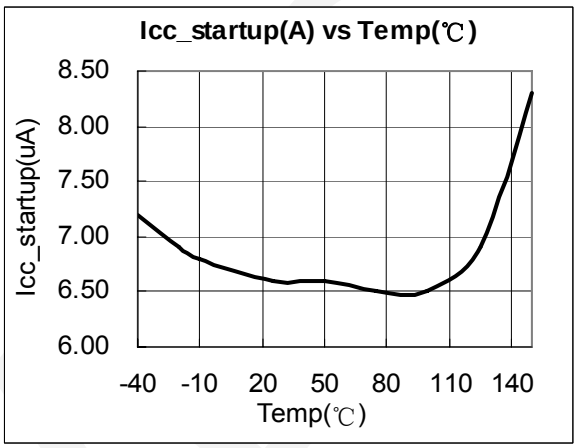
TYPICAL PERFOMANCE CHART

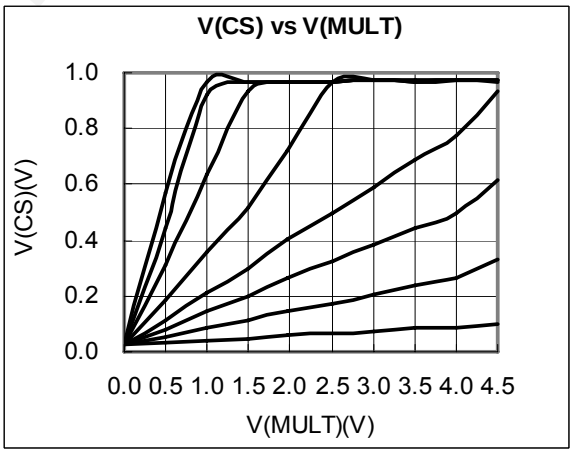












OPERATIONAL DESCRIPTION

WT6679 is a high power factor flyback PWM controller special for lighting application. The transition mode control greatly reduces the switch turn-on loss, improves the conversion efficiency and provides very good power factor correction.

- **Startup Current and Start up Control**

The typical startup current of WT6679 is 5uAwhen the VCC pin is lower than the UVLO threshold so that VCC could be charged up and start up the device. A high value, low wattage startup resistor can therefore be used to minimize the power loss during the normal operation.

- **PWM Modulator**

WT6679 employs peak current control in flyback system with power factor correction. The PWM stage compares the COMP signal (EA output) with CS pin voltage to generate PWM duty cycle. A new PWM cycle is always triggered by the Zero Current Detection (ZCD) block, and exits whenever the CS voltage exceeds COMP voltage.

- **Error Amplifier**

The inverting input of the Error Amplifier (E/A) is compared to an internal reference voltage (2.5V) to determine COMP voltage. An external loop compensation network is placed between COMP and FB. COMP is subtracted by 2.5V and then is internally connected to the multiplier input, as shown in figure 1.

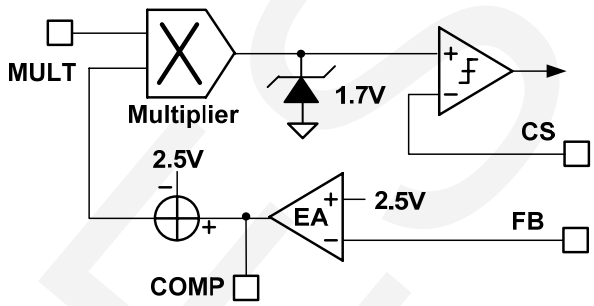


Fig.1

- **Analog Multiplier for Power Factor Correction**

The built-in analog multiplier output limits the MOSFET peak current with respect to the AC half wave rectified input voltage. Through controlling the CS comparator threshold as the AC line voltage traverses sinusoidally from zero to peak line voltage, the load appears to be resistive to the AC line and near to unity power factor can be achieved. In WT6679, the two inputs for the multiplier are designed to achieve good linearity over a wide dynamic range to represent an AC line free from distortion. Special efforts have been made to assure universal line applications with respect to a 90 to 264 VAC range. The multiplier output is internally clamped to 1.0V, as shown in Fig.1.

- **Current Sensing Comparator and Leading Edge Blanking**

Cycle-by-Cycle current limiting is offered in WT6679. The switch current is detected by asense resistor into the sense pin. An internal leading edge blanking circuit chops off the sense voltage spike at initial MOSFET on state due to Snubber diode reverse recovery so that the external RC filtering on sense input is no longer required. The current limit comparator is disabled and thus cannot turn off the external MOSFET during the blanking period. PWM duty cycle is determined by the current sense input voltage and COMP pin voltage.

- **Zero Current Detection**

WT6679 performs zero current detection (ZCD)by monitoring the voltage activity on the auxiliary windings through ZCD pin in series with an external resistor. This voltage features a flyback polarity. When the stored energy of the flyback transformer is fully released to the output, the voltage at ZCD pin decreases. When ZCD pin voltage falls below 0.25V, an internal ZCD comparator is triggered and a new PWM switching cycle is initiated following the ZCD triggering. If no zero current triggering signal is detected on ZCD pin, the “Startup Timer” block in WT6679 will generate a restart signal in 55 usec (typ.) after the last PWM signal. The maximum and minimum voltage of ZCD pin is internally clamped to 5.8V and 0V respectively.

- **Gate Drive Output**

The output stage is designed to ensure zero cross-conduction current. This minimizes heat dissipation, increase efficiency, and enhance reliability. The output driver is also slew rate controlled to minimize EMI. The built-in 16V clamp at the gate output protects the MOSFET gate from high voltage stress.

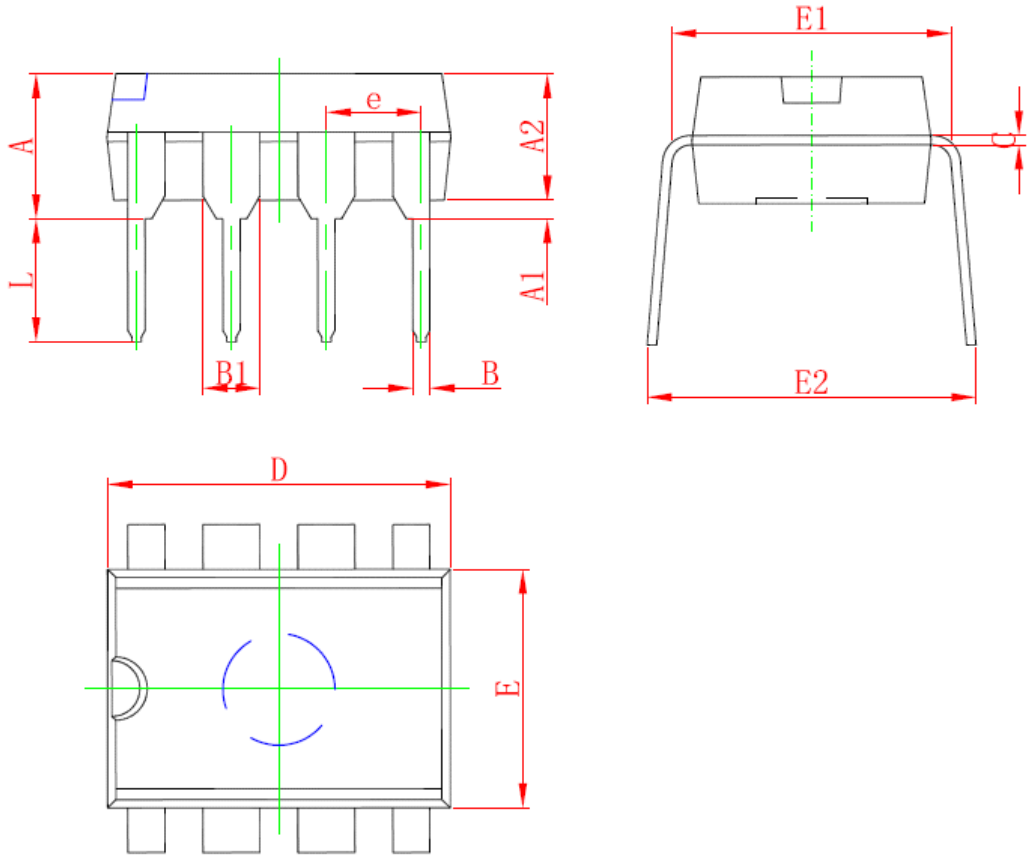
- **Protection Controls**

WT6679 ensures good reliability design throughits good protection coverage. VCC under voltage lockout (UVLO), VCC over voltage protection(auto recovery), Cycle-by-cycle current limiting and output gate clamp are standard features provided by WT6679.

PACKAGE MECHANICAL DATA

8-Pin Plastic DIP

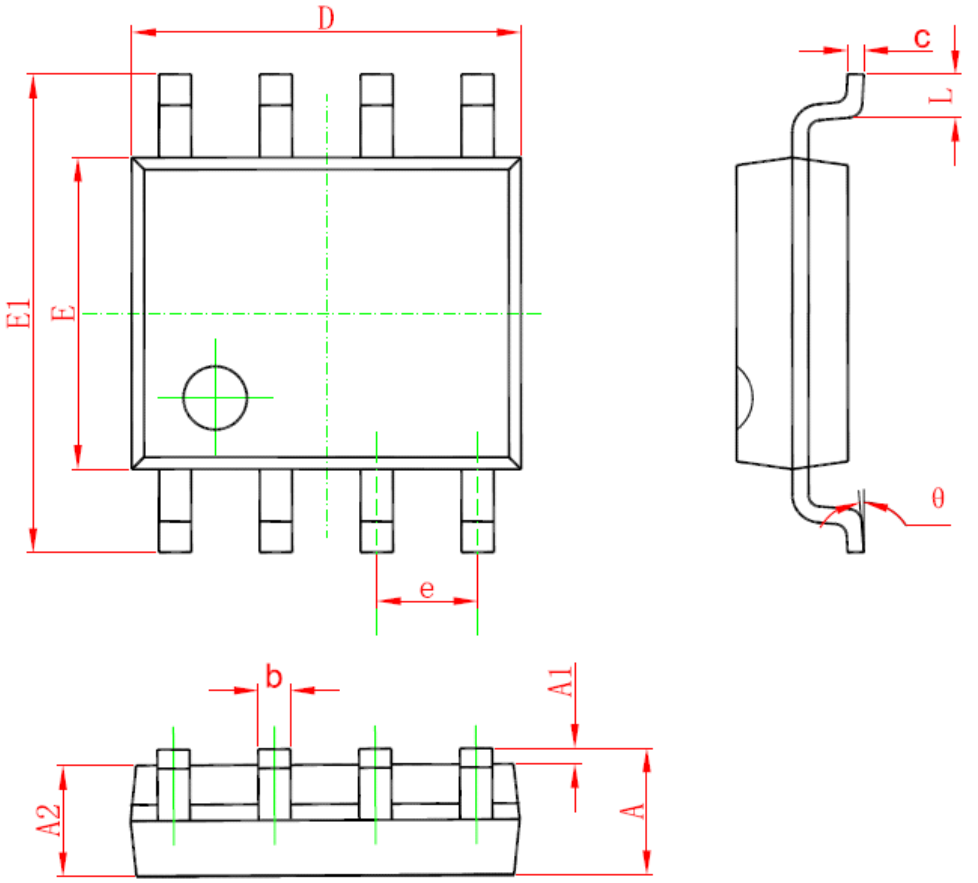
DIP8 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	5.334	0.146	0.210
A1	0.381		0.015	
A2	3.175	3.600	0.125	0.142
B	0.350	0.650	0.014	0.026
B1	1.524 (BSC)		0.06 (BSC)	
C	0.200	0.360	0.008	0.014
D	9.000	10.160	0.354	0.400
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540 (BSC)		0.1 (BSC)	
L	2.921	3.810	0.115	0.150
E2	8.200	9.525	0.323	0.375

8-Pin Plastic SOP

SOP8 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.650	0.049	0.065
b	0.310	0.510	0.012	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.150	0.185	0.203
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.05 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°