FEATURES

- Power on Soft Start Reducing MOSFET V_{DS} Stress
- Frequency shuffling for EMI
- Extended Burst Mode Control For Improved Efficiency and Minimum Standby Power Design
- Audio Noise Free Operation
- Fixed 65kHz Switching Frequency
- Comprehensive Protection Coverage
- VDD Under Voltage Lockout with Hysteresis (UVLO)
- Cycle-by-Cycle Over Current Threshold
- Overload Protection (OLP) with auto-recover
- Over Temperature Protection (OTP) with auto-recovery
- VDD Over voltage Protection(OVP) with auto-recovery
- Ultra low standby current for energy star specification 6.0

APPLICATIONS

Offline AC/DC fly-back converter for

- Battery Charger
- Power Adapter
- Set-Top Box Power Supplies
- Open-frame SMPS

GENERAL DESCRIPTION

WT8363B is a highly integrated current mode PWM control IC optimized for high performance, low standby power and cost effective offline fly-back converter applications.

PWM switching frequency at normal operation is internally fixed and is trimmed to tight range. At no load or light load condition, the IC operates in extended ‘burst mode’ to minimize switching loss Lower standby power and higher conversion efficiency is thus achieved.

VDD low start-up current and low operating current contribute to a reliable power on start-up and low standby design with WT8363B.

WT8363B offers complete protection coverage with auto-recovery including Cycle-by-Cycle current limiting (OCP), Over Load Protection (OLP), Over Temperature Protection (OTP), Over Voltage (fixed or adjustable) Protection (OVP) and VDD Under Voltage Lockout (UVLO).

Excellent EMI performance is achieved. Frequency shuffling technique. The tone energy at below 20kHz is minimized in the design and audio noise is eliminated during operation.

WT8363B is offered in SOT23-6 package.

TYPICAL APPLICATION

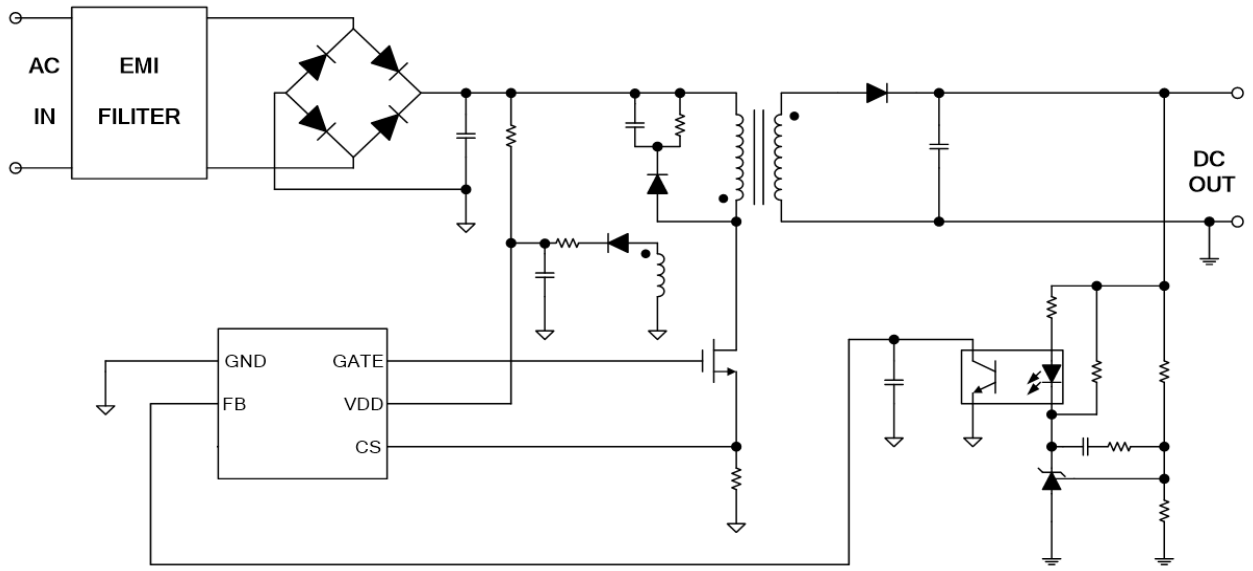
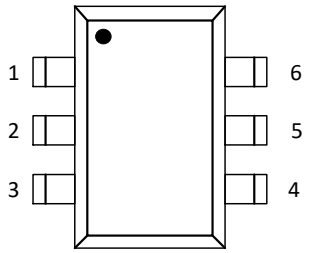


Figure 1. Basic Application Circuit

PACKAGE/ORDER INFORMATION

	Order Part Number	Package	Top Marking
	WT8363B	SOT23-6	63G13YWW

PIN DESCRIPTION

Pin Name	Pin Number	I /O	Description
GND	1	P	Ground pin.
FB	2	I	Feedback input pin. The PWM duty cycle is determined by voltage level into this pin and the current-sense signal at Pin4.
NC	3	-	NC
CS	4	I	Current sense input
VDD	5	P	Power Supply
GATE	6	O	Totem-pole gate driver output for power MOSFET

ABSOLUTE MAXIMUM RATINGS (Note 1)

Parameter Value	Range	Unit
VDD Voltage	45	V
FB Input Voltage	-0.3~7	V
Sense Input Voltage	-0.3~7	V
RT Input Voltage	-0.3~7	V
Min/Max Operating Junction Temperature TJ	-40 to 150	℃
Min/Max Storage Temperature TSTG	-40 to 160	℃
Lead Temperature (Soldering, 10secs)	300	℃

Note: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

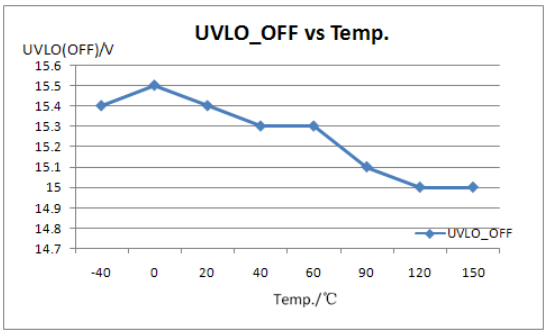
ELECTRICAL CHARACTERISTICS (Note 2)

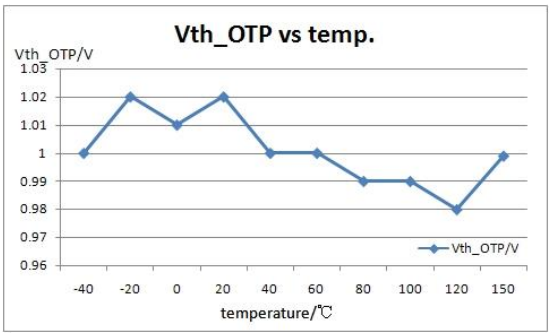
(T_A = 25°C,VDD=18V, unless otherwise noted.)

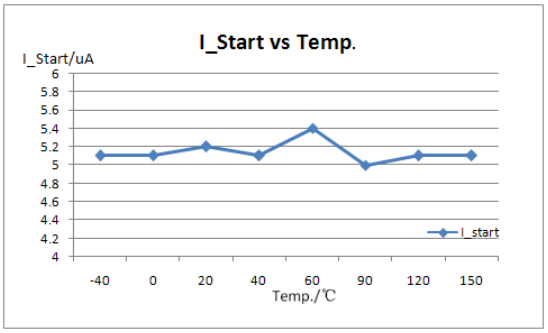
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage (VDD)						
$I_{STARTUP}$	VDD Start up Current	VDD=UVLO(OFF) -		5	20	μA
I_VDD_Operation	Operation Current	VDD=18V,V_{FB}=3V ,		1.6	2.5	mA
UVLO(ON)	VDD Under Voltage Lockout Enter		6.5	7.5	8.5	V
UVLO(OFF)	VDD Under Voltage Lockout Exit (Recovery)		19	21	23	V
OVP(ON)	Over voltage protection voltage		40	42	44	V
Feedback Input Section(FB Pin)						
VFB_Open	VFB Open Loop Voltage		3.9			V
Avcs	PWM input gain Δ V_{FB}/ Δ V_{CS}			2		V/V
Maximum duty cycle	Max duty cycle @ VDD=18V,V_{FB}=3V,V_{CS}=0V		75	80	85	%
Vref_green	The threshold enter green mode			2		V
IFB_Short	FB pin short circuit current			0.35		mA
VTH_PL	Power Limiting FB Threshold Voltage			3.7		V
Current Sense Input(CS Pin)						
SST	Soft start time			4		mS
T_blanking	Leading edge blanking time			250		nS
ZSENSE_IN	Input Impedance			40		kΩ
TD_OC	Over Current Detection and Control Delay			120		nS
VTH_OC	Internal Current Limiting Threshold Voltage with zero			0.77		V
Vocp_clamping	CS voltage clamper			1.0		V
Oscillator						
F_{OSC}	Normal Oscillation Frequency		60	65	70	kHZ

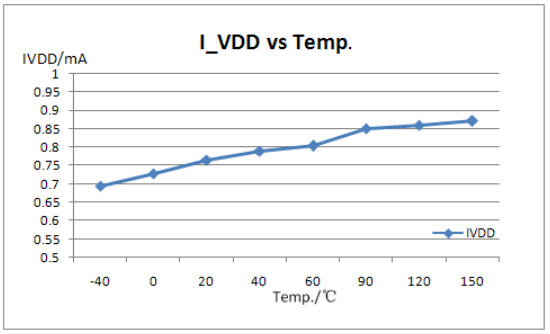
△f_OSC	Frequency jittering		±4		%
F_shuffling	Shuffling frequency		32		Hz
△f_Temp	Frequency Temperature Stability		1		%
△f_VDD	Frequency Voltage Stability		1		%
F_Burst	Burst Mode Switch Frequency		22		kHz
Gate driver					
VOL	Output low level @Output VDD=18V,Io=5mA			1	V
VOH	Output high level @VDD=18V, Io=20mA	6			V
V_clamping	Output clamp voltage		10		V

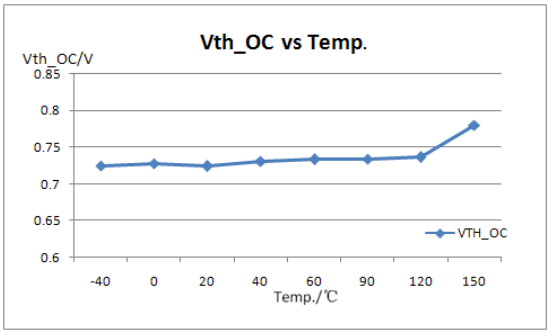
TYPICAL PERFORMANCE CHARACTERISTICS

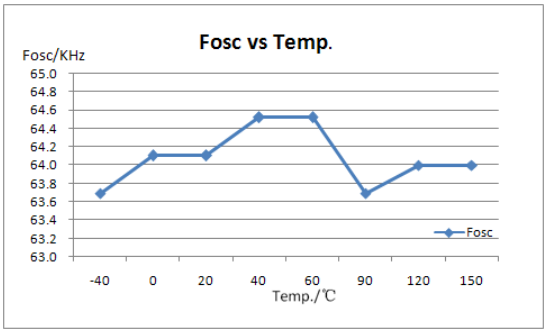












FUNCTIONAL BLOCK DIAGRAM

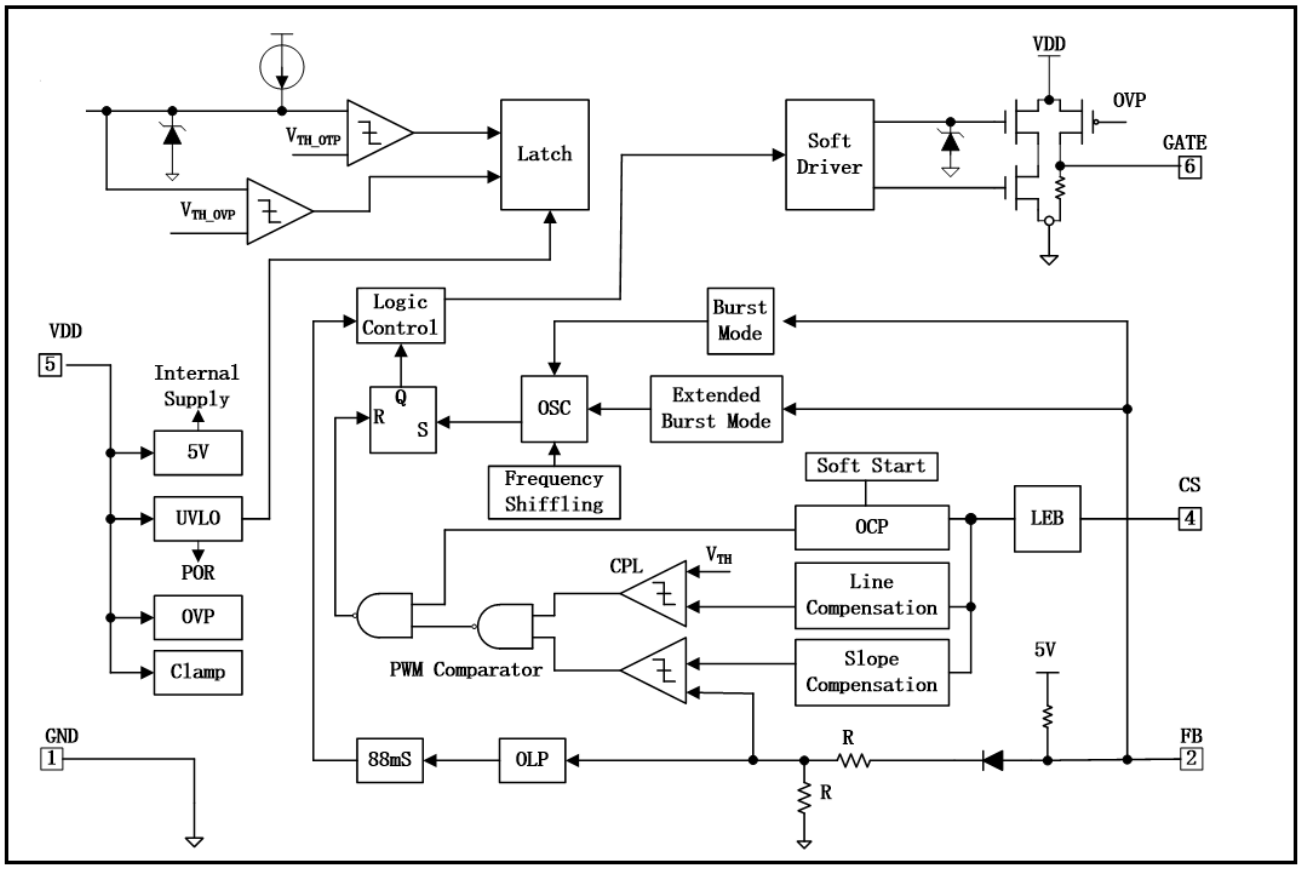


Figure 2. WT8363B Block Diagram

PERATION DESCRIPTION

WT8363B is a highly integrated current mode PWM control IC optimized for high performance, low standby power and cost effective offline fly-back converter applications. The ‘Extended burst mode’ control greatly reduces the standby power consumption and helps the design easily to meet the international power conservation requirements.

Start up Current and Start up Control

Start up current of WT8363B is designed to be very low so that VDD could be charged up above UVLO threshold level and device starts up quickly.A large value start-up resistor can therefore be used to minimize the power loss yet achieve a reliable start-up in application.

Operating Current

The Operating current of WT8363B is low at 1.8mA.Good efficiency is achieved with WT8363B low operating current together with the ‘Extended burst mode’ control features.

Soft Start

WT8363B features an internal 4ms soft start to soften the electrical stress occurring in the power supply during start-up. It is activated during the power on sequence. As soon as VDD reaches UVLO(OFF), the CS peak voltage is gradually increased from 0.05V to the maximum level. Every restart up is followed by a soft start.

Frequency shuffling for EMI improvement

The frequency Shuffling (switching frequency modulation) is implemented in WT8363B. The oscillation frequency is modulated so that the tone energy is spread out. The spread spectrum minimizes the conduction band EMI and therefore eases the system design.

Extended Burst Mode Operation

At light load or zero load condition, most of the power dissipation in a switching mode power supply is from switching loss on the MOSFET, the core loss of the transformer and the loss on the snubber circuit. The magnitude of power loss is in proportion to the switching frequency. Lower switching frequency leads to the reduction on the power loss and thus conserves the energy. The switching frequency is internally adjusted at no load or light load condition. The switch frequency reduces at light/no load condition to improve the conversion efficiency. At light load or no load condition, the FB input drops below_burst_L (the threshold enter burst mode) and device enters Burst Mode control. The Gate drive output switches when FB input rises back to Vref_burst_H (the threshold exit burst mode).Otherwise the gate drive remains at off state to minimize the switching loss and reduces the standby power consumption to the greatest extend.The switching frequency control also eliminates the audio noise at any loading conditions.

Oscillator Operation

The switching frequency is internally fixed at 65kHz.No external frequency setting components are required for PCB design simplification.

Current Sensing and Leading Edge Blanking

Cycle-by-Cycle current limiting is offered in WT8363B current mode PWM control. The switch current is detected by a sense resistor into the CS pin. An internal leading edge blanking circuit chops off the sensed voltage spike at initial internal power MOSFET on state due to snubber diode reverse recovery and surge gate current of power MOSFET. The current

limiting comparator is disabled and cannot turn off the internal power MOSFET during the blanking period. The PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

Internal Synchronized Slope Compensation

Built-in slope compensation circuit adds voltage ramp onto the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

Drive

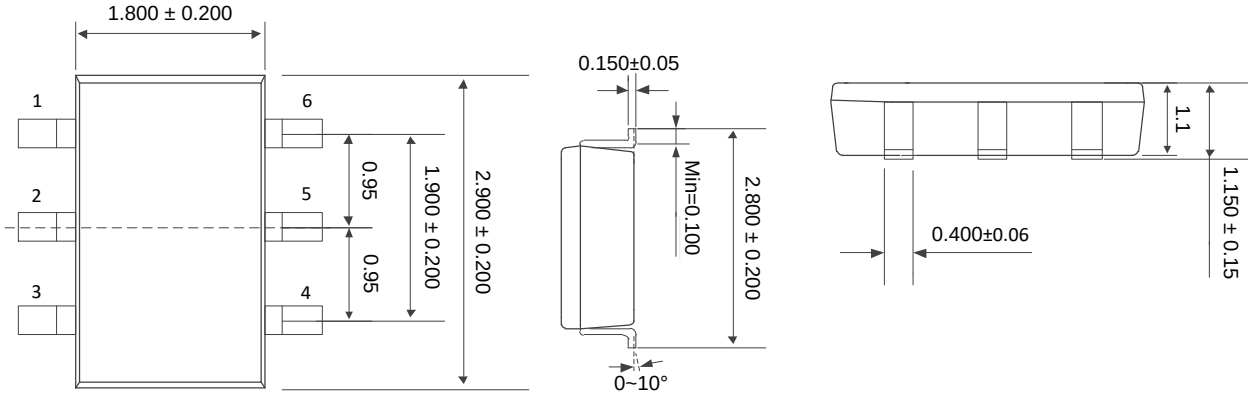
The power MOSFET is driven by a dedicated gate driver for power switch control. Too weak the gate drive strength results in higher conduction and switch loss of MOSFET while too strong gate drive results the compromise of EMI.A good trade-off is achieved through the built-in totem pole gate design with right output strength and dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme.

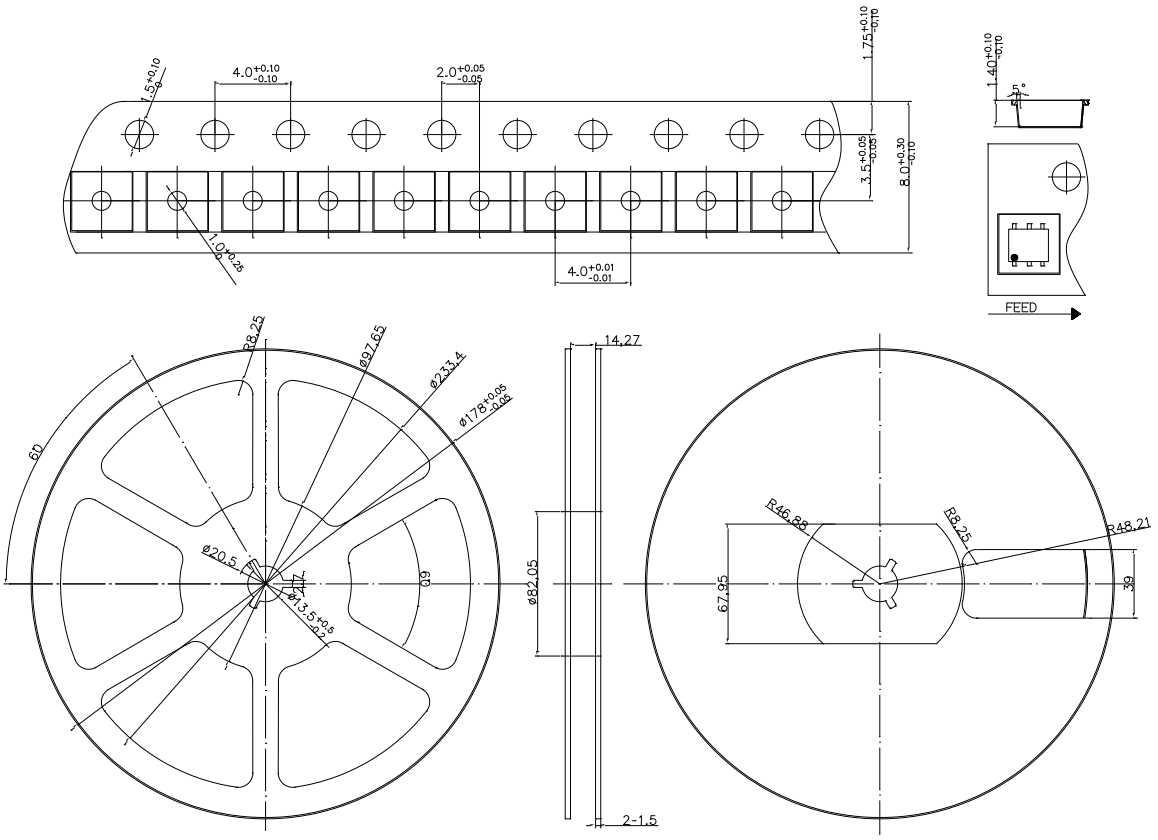
Protection Controls

Good power supply system reliability is achieved with auto-recovery protection features including Cycle-by-Cycle current limiting (OCP), Over Load Protection (OLP), and Under Voltage Lockout on VDD (UVLO), and auto-recovery shutdown features including over temperature protection (OTP), fixed or adjustable VDD over voltage protection (OVP). With Aerosemi technology, the OCP is line voltage compensated to achieve constant output power limit over the universal input voltage range. At overload condition when FB input voltage exceeds power limit threshold value for more than TD_PL, control circuit reacts to shut down the converter. It restarts when VDD voltage drops below UVLO limit. For protection with auto-recovery mode, control circuit shutdowns the power MOSFET when an Over Temperature condition or Over Voltage condition is detected until VDD drops below 9V (UVLO on voltage) , and device enters power on restart-up sequence thereafter.

PACKAGE DESCRIPTION

SOT23-6





Note:

1. All dimensions are in millimeters;
2. The pad color is silver.